IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method of fault resilient booting in a multiprocessor system, comprising:

designating one processor as a bootstrap processor;

providing a reset signal that starts a watchdog timer timing;

testing the bootstrap processor to verify that it will run BIOS code;

setting a latch for disabling said bootstrap processor if the testing indicates a failure to run BIOS code or if the watchdog timer times out;

starting a control unit timer for providing a time limit for a power on self-test;

testing during [[a]] the power on self-test the operation of said bootstrap processor;

testing during a built-in self-test the operation of said bootstrap processor;

setting a latch for disabling said bootstrap processor if the control unit timer times out;

assigning the bootstrap process to another processor if said bootstrap processor fails a test;

said testing steps being implemented in an appliance server management system.

2. (Currently Amended) The method according to claim 1, wherein testing the bootstrap processor to verify that it will run BIOS code comprises using [[a]] the watchdog timer ~~which indicates~~ to indicate a failure if the bootstrap processor is not reset within a predetermined time.

3. (Original) The method according to claim 2, wherein a failure in the second or third testing step also causes said latch to be set.

4. (Original) The method according to claim 1, wherein the testing steps are controlled by a control unit.

5. (Original) The method according to claim 4, wherein the control unit includes the system I/O chip.

6. (Currently Amended) An apparatus for fault resilient booting, comprising:

a first processor designated as a bootstrap processor;

a latch including a set input and a reset input, and including an output coupled to said bootstrap processor for turning off said bootstrap processor;

a control unit including a timer coupled to the set input for providing a first control signal ~~signals~~ for setting said latch, the control unit including a second control signal coupled to the reset input for resetting said latch, and at least one additional control signal for controlling additional processors;

a watchdog timer coupled to the set input for setting said latch, wherein the control unit includes a third control signal coupled to a reset input of the watchdog timer for resetting the watchdog timer.

7. (Currently Amended) The apparatus according to claim 6, further comprising [[a]] the reset input of the watchdog timer coupled to the output of the watchdog timer through one or more logic gates ~~for determining if said bootstrap processor is operating properly~~.

8. (Currently Amended) The apparatus according to claim 7, wherein said watchdog timer begins a time period wherein power is turned on and ends said time period after a predetermined time.

9. (Currently Amended) The apparatus according to claim 8, wherein the bootstrap processor is considered to fail if said watchdog timer is not reset before reaching said predetermined time.

10. (Original) The apparatus according to claim 6, wherein said control unit includes a system I/O chip.

11. (Original) The apparatus according to claim 6, wherein the apparatus is part of an appliance server management system.

12. (Currently Amended) A multiprocessor system for fault resilient booting, comprising:

a plurality of processors with one processor being designated a bootstrap processor;

a control unit including a timer, the control unit operable for generating a ~~series~~ plurality of control signals;

a watchdog timer including a watchdog timer reset input coupled to a fourth of the plurality of control signals;

a latch including a set input, a reset input, and a latch output, the set input coupled to an output of the watchdog timer and to a first of the plurality of control signals, the reset input coupled to a second of the plurality of control signals, and the latch output coupled to said bootstrap processor for turning said bootstrap processor off;

said watchdog timer providing a signal indicating that a predetermined time has expired, which is applied to said latch to set said latch;

said control unit providing [[a]] the first control signal to said latch for setting said latch, [[a]] the second control signal applied to said latch for resetting said latch, a third control signal for controlling other processors and [[a]] the fourth control signal for resetting the watchdog timer.

13. (Currently Amended) The system according to claim 12, wherein said first control signal from said control unit is generated when said bootstrap processor fails a power-on self-test or a built-in self-test.

14. (Currently Amended) The system according to claim 12, wherein said watchdog timer tests whether said bootstrap processor can run BIOS code.

15. (Original) The system according to claim 12, wherein the system is part of an appliance server management system.

16. (Previously Presented) A system according to claim 12, wherein said control unit causes another processor to become the bootstrap processor when said bootstrap processor is disabled by said latch.